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(54) PIXEL ARRAY HAVING IMAGE FORMING PIXEL ELEMENTS INTEGRAL WITH PERIPHERAL CIRCUIT ELEMENTS

PIXELANORDNUNG, WELCHE DIE BILDERZEUGENDEN PIXELELEMENTE INTEGRAL MIT DEN PERIPHEREN SCHALTKREISELEMENTEN HAT

MATRICE DE PIXELS A ELEMENTS DE FORMATION D'IMAGE SOLIDAIRES D'ELEMENTS DE CIRCUITS PERIPHERIQUES

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Description

FIELD OF THE INVENTION

The invention relates generally to pixel arrays and, more particularly, it relates to imager or display pixel arrays having individual pixel elements which include extra configurable transistors that can be interconnected to form the circuitry necessary to implement peripheral functions such as amplifiers and switches.

BACKGROUND OF THE INVENTION

Current imaging devices such as Computer Automated Tomography (CAT) scanners typically use imager arrays in order to detect x-rays. A typical imager arrays generally consist of a matrix of picture element (pixel) sensors which employ photodetectors to detect the light emitted by a scintillation material, which has been excited by an x-ray, and a charge storage device (e.g., capacitor) to hold an amount of charge which depends on the intensity of the detected light.

In addition to the pixel elements in the imager arrays, other peripheral circuitry is typically used to access and read the charge held by individual capacitors. The other circuitry typically includes vertical and horizontal scanning circuits, amplifiers and switches. A major problem with this peripheral circuitry is that it consumes precious space on the imager arrays which could otherwise be used for light detection circuitry. The less light detection circuitry, the less accurate and precise are the detection readings. The space on the array which cannot detect light is known as dead space.

Examples of prior art imagers having dead space for the implementation of scanning circuitry include U.S. Patent No. 5,184,018 (Conrads et al.) and U.S. Patent No. 5,115,293 (Murayama et al.). Conrads discloses a light or x-ray sensitive sensor array in which each sensor has a photodetector in parallel with a storage capacitor which is serially connected with a switching FET. Conrads also discloses amplifiers, an analog multiplexer and a digital encoder all of which are separate from the sensor elements and implemented in the marginal area of the array. Murayama discloses an imaging device having a photodetector which is serially connected to two switching MOS transistors. Murayama also discloses a vertical scanning circuit and a horizontal scanning circuit separate from the pixel elements and implemented in the marginal area of the array.

European Patent Application 0 046 396 discloses a pixel array with a plurality of select lines, a plurality of signal lines, a phototransducer means a switching means coupled between one of the plurality of signal lines. The switching means is responsive to signals on one of the plurality of select lines. Each pixel cell also includes a three transistor circuit which is used to amplify the signal produced by the pixel cell and reset the pixel cell in a predetermined cycle.

European Patent Application 0 253 391 discloses a plurality of photocells two-dimensionally arranged. Each photocell is connected to a first and second sum signal output line. Each pixel cell includes a single transistor variable gain amplifier.

International Patent Application WO 93/04384 discloses a scintillator for converting impinging x-rays into visible light, a sensor array having two opposed surfaces, a plurality of detectors and a plurality of processing circuits. The scintillator includes a lumped-circuit gain stage in close proximity to the sensors.

In view of the disadvantages (e.g., increased size of the sensor) caused by dead space circuitry, it would be advantageous to have an imager array which provides, for examples, amplifiers and scanning circuits but minimizes the amount of dead space on the array in order to maximize the accuracy and precision of the light detection readings

The present invention involves a pixel array which includes an array of image pixel elements, a plurality of select lines, and a plurality of signal lines. Each pixel element includes a phototransducer device which either senses light, modulates light or emits light. Each pixel element further includes a switching device coupled between the phototransducer device and a predetermined signal line. The switching device responds to signals on a selected select line to convey signals between the photo-transducer device and the predetermined signal line. Finally, the pixel element includes at least one configurable transistor the configurable transistor is independent of the switching device. Within the pixel array, the individual configurable transistors of the various pixel elements have multiple terminals which are coupled together by connection devices in order to implement arbitrary multitransistor circuits which are distributed across the pixel array.

BRIEF DESCRIPTION OF THE DRAWING

The invention is best understood from the following detailed description when read in connection with the accompanying drawings, in which:

Fig. 1 shows a schematic representation of a single pixel element having at least one extra transistor;
Fig. 2 is a side view of the pixel element of Fig. 1;

Fig. 3 is a top view of the pixel element of Fig. 1:

Fig. 4 shows a schematic representation of several pixel elements configured for different functions:

Fig. 5 shows a layout of a pixel element of Fig. 4 suitable for implementing a reset function;

Fig. 6 shows a layout of a pixel element of Fig. 4 suitable for implementing an amplifier function;

Fig. 7 shows a layout of a pixel element of Fig. 4 suitable for implementing an analog switch function;

Fig. 8 shows a layout of the pixel element of Fig. 4 suitable for implementing an inverter function;

Fig. 9 shows a schematic representation of a basic shift register element comprising a plurality of extra transistors from pixel elements such as that shown in Fig. 1;

Fig. 10 shows a schematic representation of a partial interconnection layout of several shift register elements such as those shown in Fig. 9:

Fig. 11 shows an image sensor formed as a matrix of 20 imager arrays each formed from pixel cells such as that shown in Fig. 1;

Fig. 12 is a side-view of the image sensor shown in Fig. 11 which is useful for describing a packaging scheme for the image sensor; and

Fig. 13 is a detail view of the image sensor shown in Fig. 12 which is useful for describing a packaging scheme for the image sensor.

DETAILED DESCRIPTION OF THE INVENTION

The present invention has particular application for building both large imager or large display arrays by interconnecting many individual four-side buttable pixel arrays.

Fig. 1 shows a schematic representation of a pixel element 10 suitable for use in a pixel array. The phototransducer device in the element 10 is a photodetector 12. Photodetector 12, such as a photodiode, is implemented using an N-well to P-substrate photodetector to integrate photo-generated charge. Photodetector 12 is coupled in parallel with a capacitor 14 to increase the maximum charge handling capacity of element 10. In the exemplary embodiment, capacitor 14 is a thin-oxide (Tox) capacitor.

Coupled between photodetector 12 and a signal line (HSIG) are two series connected transistors 16 and 18. Transistors 16 and 18 are responsive to the row select line (ROW_SEL) and column select line (COL_SEL), respectively, such that when both are activated the charge of element 10 is read out to HSIG. In the exemplary embodiment, transistors 16 and 18 are NMOS transistors.

In addition to, and independent of transistors 16 and 18, one or more "configurable" transistors 20a (with optional transistor 20b) may be included in element 10. The extra transistor(s), along with similar extra transistors within each of the remaining pixel elements in the pixel array, are "configured" with polysilicon and/or metallization interconnections as necessary to form the circuitry needed to implement desirable functions. These functions may be, for example, signal line source followers, analog switches, and row and column scanning registers. These transistors may be NMOS or PMOS or a mixture of the two types.

For those functions (such as low-noise source follower amplifiers) which are desirably implemented using relatively wide transistors, a number of the extra transistors from multiple pixel elements may be connected in parallel to form a composite device having the desired device size.

Because the peripheral functions are spread over many pixel elements on a pixel array, area at the edges of the pixel array is not needed to form the above-mentioned peripheral functions (e.g., scanning registers and sense amplifiers). In prior imager designs these elements are typically implemented along the edges of the imager array. This configuration allows the pixel array to have a very small dead space (i.e., space that is not sensitive to light photons) at the edges. Accordingly, multiple imager arrays may be joined along the edges to form larger arrays. Any distortion caused by the small gaps at the joined edges may be corrected using image processing techniques. The result is a 'seamless' overall imager array using multiple component four-side buttable pixel arrays. Since each component array is made separately, the manufacturing yield of a matrix of component arrays is typically much larger than for an equivalent monolithic array. Similar techniques may be used to form image display devices.

In a typical display device, the photodetector would be replaced, for example, by a liquid crystal device (LCD) or a light emitting device, such as a light-emitting diode (LED) or other electroluminescent device. When the phototransducers are LCD's, the active components of these arrays are typically thin film transistors (TFTs). In this instance, it may be desirable to implement the extra transistors as TFTs. In any image display device, it may be desirable to interconnect these transistors to form the desired peripheral circuits using a transparent conductor such as indium-tin oxide.

Figs. 2 and 3 show layouts for the basic components of a pixel element as well as the extra transistor(s). Fig. 2 shows a side view of a layout of a basic pixel element without the extra transistor. In Fig. 2, photodetector 12 includes an N well 40 in a P substrate 42. A 1 picofarad (pF) Tox capacitor 14 is set in parallel with the layers of photodetector 12. Also, connected to N well 40 of photodetector 12, are the series transistors 16 and 18.

Fig. 3 shows a top view of a layout of the pixel element in Fig. 1. Fig. 3 shows the outline of photodetector 12 which is, in turn, coupled to series transistors 16 and 18. Two extra transistors 20a and 20b are also shown in Fig. 3.

Fig. 4 shows a schematic representation of three pairs of pixel elements having their respective extra transistor configured for 3 different functions. For purposes of clarity, only one pixel element from each pair is described below. Pixel element 210 is configured to implement a reset function. Pixel element 230 is configured to implement an amplifier function. And, pixel element 250 is configured to implement an analog switch function.

As shown, element 210 includes photodetector 212 with parallel capacitor 214. Transistors 216 and 218 are coupled in series between photodetector 212 and the horizontal signal line (HSIG). The respective gates of transistors 216 and 218 are coupled to the ROW_SEL line and the COL_SEL line such that when both select lines are active the charge of element 210 (held by capacitor 214) is read out onto HSIG.

In general, the configuration of the photodetector, capacitor and the two switching transistors are the same for each pixel element; however, it is the configuration of the extra transistor 220, 240 or 260 which changes, thereby allowing peripheral circuitry to be implemented within the pixel arrays.

In element 210, to implement the reset function, the extra transistor 220 is coupled between a signal line which conveys a source of reference potential (e.g. VDD) and HSIG such that when the RESET/VSIG line is activated and the element 210 is selected, the element 210 is reset. This resetting of element 210 is accomplished by charging the capacitor 214 to VDD with respect to ground potential. During the imaging process, when the photodetector 212 is illuminated, it will reduce the level of charge on the capacitor 214, reducing the potential with respect to ground.

A layout of element 210 suitable for use with the reset function is shown in Fig. 5. In Fig. 5, the outline of photodetector 212 includes a tab-like extension which connects with transistor 216. Transistor 216, in turn, is connected in series with transistor 218. As shown, the ROW_SEL and COL_SEL lines are connected to the gates of transistors 216 and 218 for controlling access to the state of photodetector 212 and capacitor 214 (i.e. the amount of electrical charge on the capacitor 214). The extra transistor 220 is connected between the VDD and HSIG signal lines with its gate connected to RESET/VSIG such that, when a positive pulse occurs on the RESET/VSIG line, and the transistors 216 and 218 are rendered conductive by the COL_SEL and ROW_SEL signals, the element 210 is reset.

Referring back to Fig. 4, the extra transistor 240 of pixel element 230 is configured to implement the amplifier function. Transistor 240 is coupled between the VDD and BUF_SIG signal lines and has the signal line HSIG is coupled to its gate electrode. Thus, when HSIG is active, it modulates the conductivity of transistor 240, which effectively places a buffered (i.e., amplified) version of the signal on the HSIG line onto the BUF_SIG line.

In Fig. 6 a layout of element 230 suitable for implementing the amplifier function is shown in Fig. 6 is basically the same as that for element 210. The only significant difference is how extra transistor 240 is interconnected. In Fig. 6, the drain and source electrodes of transistor 240 are connected to the signal lines VDD and BUF_SIG, respectively, while its gate electrode is connected to the signal line HSIG. In this configuration, the signal on HSIG modulates the conductivity of transistor 240 which effectively causes it to act as an amplifier. In this instance, an amplified version of the signal on HSIG (i.e., a signal having the same characteristics as HSIG) is placed on the BUF_SIG line.

Referring back to Fig. 4, in element 250, transistor 260 is coupled between the signal lines RESET/VSIG and BUF_SIG to implement the analog switch function. In this configuration, when the ROW_SEL signal line is activated, the signal on the BUF_SIG signal line is gated onto the RESET/VSIG signal line.

In Fig. 7 a layout of element 250 suitable for use with the analog switch function is basically the same as that for pixel elements 210 and 230. Again, the only significant difference is how extra transistor 260 is interconnected. In Fig. 7 the source and drain electrodes of transistor 260 are connected between the BUF_SIG and RESET/VSIG signal lines and the gate electrode is connected to the ROW_SEL signal line. In this configuration, the signal on the ROW_SEL signal line turns on transistor 260 which effectively acts as a switch by routing the signal on the BUF_SIG line onto the RESET/VSIG line from which it can then be read.

In addition to the above configurations of the extra transistors, it is also desirable to be able to implement an inverter device available, for example, to simplify the implementation of scanning circuits. In Fig. 8 a pixel element 610 includes extra transistors 622 and 624 coupled to implement a CMOS inverter circuit. In this circuit, an input signal applied to the IN line produces an inverted version of the signal on the OUT line.

In Fig. 9 a basic shift register element 710 used to implement a read out scheme has a positive potential (i.e. logic-high) at input terminal A(1) which is propagated through the transistor 712 responsive to a pulse of the clock signal PH1. An electrical charge caused by gating the potential is stored on the capacitance of the gate electrodes of the transistors which make-up the inverter circuit 714. The source of this capacitance is described below with reference to Fig. 10.

The positive potential (logic-high) at the input terminal of the inverter causes the inverter to gate its output terminal to a source of reference potential (e.g. ground) Next, in response to a pulse of a clock signal PH2, any charge stored at the input terminals of the inverters 718, 720 and 722 is drained to ground (i.e. logic-low), causing the output terminals of the inverters to become logic-high.

At the end of the pulse applied to A(1), when the input signal becomes logic-low, a pulse of the clock signal PH1

brings the input terminal of the inverter 714 logic-low, causing it to provide a logic-high signal to the input terminals of the inverters 718, 720 and 722, responsive to a pulse of the clock signal PH2. This logic-high input signal becomes a logic-low signal at the output terminals of the inverters 718, 720 and 722. The output signal of the inverter 722 propagates through the circuitry which includes the transistors 724 and 728 and the inverter circuits 726, 730, 732 and 734 in the same manner as described above with respect to the corresponding transistors 712 and 716 and inverter circuits 714, 718, 720 and 722.

A scan register for one or both of the rows and columns of the pixel array is implemented by connecting a plurality of circuits 710 in series with the A(2) output of one circuit coupled to the A(1) input of the next circuit. The drive lines for the respective rows or columns are the output lines OUT1 and OUT2.

In circuit 710, the inverters 718 and 719 are coupled in parallel to provide sufficient current to drive a row or column line of the display device. The exemplary clock signals PH1 and PH2 are two mutually exclusive phases of a single multi-phase clock signal. The frequency of this signal is desirably much greater than the scanning frequency of the pixel array.

In Fig. 10 a partial layout of several interconnected shift register elements includes only a portion of a row-scan shift register and a corresponding portion of a column-scan shift register are shown. The circuit elements 712 through 734 implement the same circuit as the corresponding elements of Fig. 9. In Fig. 10, each circuit element is implemented in a respectively different imaging cell of the matrix 810 as indicated by the broken lines. For example transistor 712 is implemented in imaging cell 812 while inverter 714 is implemented in cell 814.

It is noted that the input signal lines to the inverters, for example inverter 714 are relatively long. The capacitance of these lines augments the input capacitance to the inverters, allowing electrical charge to be stored on the input terminals of the respective inverters in the time between the clock phase PH1 and PH2.

The invention concerns an imaging device comprising a plurality of pixel arrays with means for coupling multiple ones of the pixel arrays to form the imaging device. The arrays comprise a plurality of configurable pixel elements for minimizing space in the array which is not occupied by pixel elements, each of the plurality of configurable pixel elements comprising phototransducer means, switching means coupled between the phototransducer means and one of the plurality of signal lines; wherein the switching means is responsive to signals on one of the plurality of select lines for conveying signals between the phototransducer and the one signal line, at least one configurable transistor, the configurable transistor being independent of the switching means, and means for coupling a plurality of configurable transistors on a respective plurality of pixel elements to form the peripheral circuitry within the array of pixel elements. The configurable pixel elements comprise photodetector means for detecting light and for holding a charge associated with the detection, select means for conveying a signal related to a held charge from a pixel element to circuits external to the imaging array, means, coupled to the photodetector means and responsive to the select means, for allowing access to a held charge, at least one configurable transistor independent of the select means, and means for coupling the configurable transistor to a plurality of other configurable transistors from other ones of the configurable pixel elements in order to form peripheral circuitry within the imaging array.

Figs. 11, 12 and 13 show a packaging scheme for an imager array including multiple four-side buttable pixel arrays. In Fig. 11, 20 (4x5) pixel arrays 920 are shown mounted on a glass plate 922. The pixel arrays are interconnected with X and Y traces 926 and 928 set out on the glass plate 922. Fig. 12 shows a side view of multiple pixel arrays mounted on glass plate 920 and being hermetically sealed. Fig. 13 shows an enlarged section of Fig. 12 particularly detailing the X and Y traces, 926 and 928, which include solder bumps for connecting to the pixel array modules. Also shown is the insulating dielectric 924 which separates the horizontally-oriented X traces 926 from the vertically-oriented Y traces 928.

In Fig. 13, the pixel arrays consist of silicon wafers 924 epoxied to a glass substrate 925 (preferably, phosphor-coated glass substrates). Prior to securing the silicon wafer containing the pixel elements to the glass substrate, however, the silicon wafer is thinned from the backside to approximately 15 um near the P^+ to P^- boundary. It should be noted that back-side implanting should not be necessary to control the backside surface recombination velocity. The 550 nm wavelength should provide adequate quantum efficiency.

The thinned silicon wafers 924 are then epoxied to the glass substrate 925. After cutting the glass substrate into tiles, the tiles are flipped and indium bump bonded to a printed circuit carrier. The backside of the original silicon wafer 924 bonded to the glass plate 925 is now the top surface of the printed circuit carrier and acts as the imaging side of the device This is illustrated in Figs. 12 and 13.

In the present invention, each pixel array (or tile) is implemented using a CMOS single-polysilicon gate, double-level metal process. One of ordinary skill in the art of fabricating semiconductor imaging arrays would recognize this as a standard foundry process. A P^- type epitaxial layer having a thickness of approximately 15um on a P^+ type substrate is used. A tile may include approximately 250x250 pixels depending on the yield with each pixel element being approximately 85 um x 85 um.

Additionally, each tile is four-side buttable with a gap of less than 20 um at the butt edge. As mentioned, the pixel elements extend to the edge of the tile with the scan registers, signal amplifiers and multiplexers built using the extra

configurable devices. The edge of each tile is sealed using a P^+ and metal contact to the P^- substrate in order to avoid any unpassivated junctions along the edge of the tile.

Some device design criteria for a pixel array are as follows:

Signal Line Capacitance Components

1. N^+ to P^- substrate (Vpn = -3V)

   Ca = 0.31 fF/ μm^2 @ OV
   Ca = 0.16 fF/ μm^2 @ -3V Area = 16 μm^2 Ca = 2.6 fF
   Cp = 0.2 fF/ μm @ OV
   Cp = 0.17 fF/ μm @ -3V Per = 12 μm Cp = 2.0 fF
   mj = 0.5 msj = 0.1

2. Cgd overlap for Q2 drain
   (Col_Select NMOS Device)
   Cp = 0.25 fF/ μm Per = 4.0 μm Cp = 1.0 fF

3. Poly to Field
   Wpoly = 2 μm
   Ca = .06 fF/ μm^2 Area = 40μm^2 Ca = 2.4 fF
   Cp = .05 fF/ μm Per = 40 μm Cp = 2.0 fF

4. Metal1 to Field
   Wml = 3.0 μm
   Ca = .04 fF/ μm^2 Area = 260μm^2 Ca = 10.4 fF
   Cp = .048 fF/ μm Per = 170 μm Cp = 8.2 fF

5. Metal1 to Metal2
   Wm2 = 3.0 μm
   Ca = .035 fF/ μm^2 Area = 9.0 μm^2 Ca = 0.3 fF
   Cp = .048 fF /μm Per = 12.0 μm Cp = 0.6 fF

   Total Signal Line Cap / pixel C/pixel = 29.5 fF
   Total Cl for 50 pixel line: Cl = 1.5 pF

6. Signal_Line source follower gate input capacitance.
   Cg = 1.0 fF/ μm^2 (Cox = 350A)
   Cgd overlap = 0.25 fF/ μm
   W = 200 μm L = 1.0 μm Av = 0.85
   Cin = 200 μm x 2.0 μm x [(1-Av)x0.67 + 0.33]x1.0 fF/ μm^2
   + 200 μm x 0.25 fF/ μm = 0.22 pF

TOTAL Signal_Line Capacitance Ctot = Cl + Cin

Ctot = 1.5 pF + 0.22 pF = 1.72 pF

Dynamic Range Components

Pixel Voltage Swing for 40M e-signal, photodetector Cpx = 1.5 pF

$$dVpx = Qpx/Cpx = 4.3\ V$$

Output Signal_Line Voltage

$$dVsig = Qpx / (Cpx+Ctot) = 2.0V$$

Pixel kTC Noise Limit

$$Vnpx = 400/1.5 = 490e\text{- rms @ } 25C$$

Source Follower Noise Estimate (W=200 μm, L=2 μm, Ids = 2mA, BW = 5MHz)
Vnt = 3nV /Hz (transistor equivalent input noise level)
Vn = 6.7 μV
Qn = 2.16E-17C = 135e-

Total RMS Readout Noise Level

$$Qntot = 508e\text{-}$$

Linear Dynamic Range (Peak Signal to RMS Noise).

$$S/N = 40Me\text{-}/508e\text{-} = 78{,}740\ (98\ dB)$$

The invention can be applied to an imaging device comprising a imager array of the invention with an associated means for generating light when excited by electromagnetic radiation of a different wavelength such as x-rays or gamma rays, such as a scintillation material. The scintillation material preferably overlies a surface of the imaging array in close proximity to the photodetectors of the pixel arrays. The scintillation material may be a uniform body of material or subdivided corresponding in size to the pixel arrays which make up the imager array or smaller dimensions to reduce the spreading of the scintillation radiation and improve imager resolution. A suitable scintillation material for detecting x-rays is gadolinium oxysulphide: europium, gadolinium oxide: europium and lanthanum oxide bromide ; terbium. The output wavelength of the scintillation material is preferably matched to the detector sensitivity.

It should be noted that although the present invention is described in an imager pixel array application, the present invention can also be used in a display pixel array application. Display arrays experience the same problems as do imager arrays in that circuitry is needed to access the pixel elements which, rather than detecting light, modulate or emit light in order to produce an overall large display picture. Thus, the present invention is useful in conjunction with any type of phototransducer element which either detects or transmits light which has application in an array device.

Although the invention is illustrated and described herein embodied as an imager pixel array in which each pixel element typically includes at least one extra configurable device, the invention is nevertheless not intended to be limited to the details as shown.

Claims

1. A pixel array (10) comprising:

   a plurality of select lines (ROW_SEL, COL_SEL);
   a plurality of signal lines (HSIG);

an array of pixel elements, each pixel element including

a phototransducer (12);

switching means (16, 18) coupled between the phototransducer and one of said plurality of signal lines; wherein the switching means is responsive to signals on one of the plurality of select lines for conveying signals between the phototransducer and the one signal line: CHARACTERIZED IN THAT the array further comprises:

a plurality of configurable transistors consisting of at least one configurable transistor (20) in each of a plurality of the pixel elements each configurable transistor having a plurality of terminals which terminals are adapted to establish connections among respective transistors of the plurality of configurable transistors; and

a plurality of connection devices (BUF_SIG, IN, OUT) which connect selected ones of the terminals of the plurality of configurable transistors to form a multitransistor circuit (710) which is distributed across a plurality of the pixel elements in the pixel array;

at least some of the said configurable transistors being arranged to perform functions of the multitransistor circuit which are independent of the functions of the pixel elements containing those transistors.

2. The pixel array of claim 1, wherein the plurality of select lines includes a plurality of column select lines (COL_SEL);

the switching means includes two series transistors (16,18) one of which is responsive to a selected column select line; and

the plurality of connection devices connect selected ones of the plurality of configurable transistors to implement, as said multitransistor circuit, a column select shift register (710).

3. The pixel array of claim 1 or 2, wherein the phototransducer is a photodetector (12).

4. The pixel array of claim 3, further comprising a charge storage means (14) coupled in parallel with the photodetector for holding an electrical charge having a magnitude which is determined by light intensity.

5. The pixel array of claim 1 wherein, the plurality of select lines includes a plurality of row select lines (ROW_SEL) and a plurality of column select lines (COL_SEL), the pixel array further comprises a plurality of auxiliary lines (BUF_SIG, IN, OUT);

the phototransducer is a photodetector (12);

the switching means is responsive to signals on a selected one of the row select lines and on a selected one of the column select lines for conveying signals between the photodetector and the predetermined signal line; and

the plurality of connection devices includes further connection devices which connect at least a first one of the plurality of configurable transistors (20) of said multitransistor circuit to a selected one of the said lines.

6. The pixel element of claim 5, wherein the plurality of auxiliary lines includes a buffered signal line (BUF_SIG), wherein a second one of the plurality of configurable transistors (20) is coupled between the buffered signal line and a source of reference potential (VDD), wherein the second one of the plurality of configurable transistors is responsive to the predetermined signal line such that when the predetermined signal line is asserted, the buffered signal line carries an amplified version of the signal conveyed by the predetermined signal line.

7. The pixel array of claim 5, wherein the plurality of signal lines includes a first plurality of signal lines and a second plurality of signal lines, wherein a second at least one of the plurality of configurable transistors (20) is coupled between one of the first plurality of signal lines and one of the second plurality, wherein the second at least one of the plurality of configurable transistors is responsive to the selected row select line such that when the selected row select line is asserted, the second at least one of the plurality of configurable transistors couples the one of the first plurality of signal lines to the one of the second plurality of signal lines.

8. The pixel array of claim 1 wherein the transducer is a photodetector and the pixel array further comprises:

means for holding a charge (14) representing light detected by the photodetector;

means, coupled to the means for holding the charge and responsive to the switching means, for allowing access to the held charge; and

means for coupling at least one of the plurality of configurable transistors to a plurality of other configurable transistors in order to implement, as the multitransistor circuit, peripheral circuitry which successively allows access to the held charge on respectively different ones of the plurality of pixel elements.

9. The pixel array of any one of claims 1-5, 8 wherein each pixel element includes only one configurable transistor, which is a metal-oxide semiconductor (MOS) transistor

10. The pixel array of any one of claims 1 to 8, wherein each pixel element includes two configurable metal-oxide semiconductor (MOS) transistors having opposite channel polarities.

11. The pixel array of claim 10 wherein the two configurable MOS transistors in a cell are configured as a complementary metal oxide semiconductor (CMOS) inverter and the connection devices are used to connect inverters in selected ones of the pixel elements with individual ones of the configurable transistors in other selected ones of the pixel elements to form a column select shift register.

12. A matrix of a plurality of pixel arrays (920) each as specified in any preceding claim the arrays being interconnected (926,928).

13. A matrix according to claim 12, wherein the arrays are abutted along the edges thereof.

Patentansprüche

1. Pixelarray (10) mit:

 einer Mehrzahl von Auswahlleitungen (ROW_SEL, COL_SEL),
 einer Mehrzahl von Signalleitungen (HSIG),
 einem Array aus Pixelelementen, wobei jedes Pixelelement aufweist:
 einen Photowandler (12),
 eine Schalteinrichtung (16, 18), die zwischen den Photowandler und eine der Mehrzahl von Signalleitungen geschaltet ist, wobei die Schalteinrichtung auf Signale aus einer der Mehrzahl von Auswahlleitungen anspricht, um Signale zwischen dem Photowandler und der einen Signalleitung zu transportieren, **dadurch gekennzeichnet**, daß das Array weiterhin aufweist:
 eine Mehrzahl von konfigurierbaren Transistoren, die aus zumindest einem konfigurierbaren Transistor (20) in jedem der Mehrzahl von Pixelelementen besteht, wobei jeder konfigurierbare Transistor eine Mehrzahl von Anschlüssen hat, wobei die Anschlüsse dafür ausgelegt sind, Verbindungen zwischen den jeweiligen Transistoren der Mehrzahl von konfigurierbaren Transistoren bereitzustellen, und
 eine Mehrzahl von Verbindungseinrichtungen (BUF_SIG, IN, OUT) welche ausgewählte Anschlüsse aus der Mehrzahl von konfigurierbaren Transistoren so verbinden, daß ein Multitransistorschaltkreis (710) gebildet wird, der auf eine Mehrzahl der Pixelelemente in dem Pixelarray verteilt ist,
 wobei zumindest einige der konfigurierbaren Transistoren so angeordnet sind, daß sie Funktionen des Multitransistorschaltkreises ausführen, die von den Funktionen der Pixelelemente, welche diese Transistoren enthalten, unabhängig sind.

2. Pixelarray nach Anspruch 1, wobei die Mehrzahl von Auswahlleitungen eine Mehrzahl von Spaltenauswahlleitungen (COL_SEL) aufweist,

 die Schalteinrichtung zwei in Reihe geschaltete Transistoren (16, 18) aufweist, von denen einer auf eine ausgewählte Spaltenauswahlleitung anspricht, und
 die Mehrzahl von Verbindungseinrichtungen Ausgewählte der Mehrzahl von konfigurierbaren Transistoren verbindet, um als der Multitransistorschaltkreis ein Spaltenauswahlschieberegister (710) zu verwirklichen.

3. Pixelarray nach Anspruch 1 oder 2, wobei der Photowandler ein Photodetektor (12) ist.

4. Pixelarray nach Anspruch 3, welches weiterhin eine Ladungsspeichereinrichtung (14) aufweist, die parallel zu dem Photodetektor geschaltet ist, um eine elektrische Ladung zu halten, die eine Größe hat, welche durch die Lichtintensität bestimmt wird.

5. Pixelarray nach Anspruch 1, wobei die Mehrzahl von Auswahlleitungen eine Mehrzahl von Zeilenauswahlleitungen (ROW_SEL) und eine Mehrzahl von Spaltenauswahlleitungen (COL_SEL) aufweist, wobei das Pixelarray weiterhin eine Mehrzahl von Hilfsleitungen (BUF_SIG, IN, OUT) aufweist,

der Photowandler ein Photodetektor (12) ist,
die Schalteinrichtung auf Signale auf einer Ausgewählten der Zeilenauswahlleitungen und auf eine Ausgewählte der Spaltenauswahlleitungen anspricht, um Signale zwischen dem Photodetektor und der vorbestimmten Signalleitung zu transportieren, und die Mehrzahl von Verbindungseinrichtungen weitere Verbindungseinrichtungen einschließt, die zumindest einen ersten aus der Mehrzahl von konfigurierbaren Transistoren (20) des Multitransistorschaltkreises mit einer Ausgewählten dieser Leitungen verbindet.

6. Pixelarray nach Anspruch 5, wobei die Mehrzahl von Hilfsleitungen eine gepufferte Signalleitung (BUF_SIG) aufweist, wobei ein zweiter aus der Mehrzahl von konfigurierbaren Transistoren (20) zwischen die gepufferte Signalleitung und eine Quelle eines Bezugspotentials (VDD) geschaltet ist, wobei der zweite aus der Mehrzahl von konfigurierbaren Transistoren auf die vorbestimmte Signalleitung derart anspricht, daß dann, wenn die vorbestimmte Signalleitung beansprucht ist, die gepufferte Signalleitung eine verstärkte Version des Signales trägt, welches durch die vorbestimmte Signalleitung transportiert wird.

7. Pixelarray nach Anspruch 5, wobei die Mehrzahl von Signalleitungen eine erste Mehrzahl von Signalleitungen und eine zweite Mehrzahl von Signalleitungen aufweist, wobei zumindest ein zweiter der Mehrzahl von konfigurierbaren Transistoren (20) zwischen eine aus der ersten Mehrzahl von Signalleitungen und eine aus der zweiten Mehrzahl geschaltet ist, wobei der zumindest eine zweite aus der Mehrzahl von konfigurierbaren Transistoren auf die ausgewählten Zeilenauswahlleitung derart anspricht, daß dann, wenn die ausgewählte Zeilenauswahlleitung beansprucht ist, der zumindest eine zweite aus der Mehrzahl von konfigurierbaren Transistoren die eine aus der ersten Mehrzahl von Signalleitungen mit der einen aus der zweiten Mehrzahl von Signalleitungen verbindet.

8. Pixelarray nach Anspruch 1, wobei der Wandler ein Photodetektor ist und das Pixelarray weiterhin aufweist:

eine Einrichtung für das Halten einer Ladung (14), welche dem Licht entspricht, das von dem Photodetektor erfaßt wurde,
eine Einrichtung, die mit der Einrichtung zum Halten der Ladung verbunden ist und auf die Schalteinrichtung anspricht, um einen Zugriff zu der gehaltenen Ladung zu gewähren, und
eine Einrichtung, um zumindest einen aus der Mehrzahl von konfigurierbaren Transistoren mit einer Mehrzahl aus anderen konfigurierbaren Transistoren zu verbinden, um als den Multitransistorschaltkreis einen Umfangsschaltkreis zu verwirklichen, der in erfolgreicher Weise Zugriff auf die gehaltene Ladung auf die jeweils Unterschiedlichen der Mehrzahl von Pixelelementen erlaubt.

9. Pixelarray nach einem der Ansprüche 1 bis 5 und 8, wobei jedes Pixelelement nur einen konfigurierbaren Transistor aufweist, der ein Metall-Oxidhalbleiter (MOS)-Transistor ist.

10. Pixelarray nach einem der Ansprüche 1 bis 8, wobei jedes Pixelelement zumindest zwei konfigurierbare Metall-Oxidhalbleiter (MOS)-Transistoren aufweist, die entgegengesetzte Kanalpolaritäten haben.

11. Pixelarray nach Anspruch 10, wobei die beiden konfigurierbaren MOS-Transistoren in einer Zelle als komplementäre Metalloxidhalbleiter (CMOS)-Inverter ausgestaltet sind und die Verbindungseinrichtungen verwendet werden, um die Inverter in ausgewählten Pixelelementen mit individuellen konfigurierbaren Transistoren in anderen ausgewählten Pixelelementen zu verbinden, um ein Spaltenauswahlschieberegister zu bilden.

12. Matrix aus einer Mehrzahl von Pixelarrays (920), wie sie in irgendeinem der vorstehenden Ansprüche beansprucht sind, wobei die Arrays miteinander verbunden sind (926, 928).

13. Matrix nach Anspruch 12, wobei die Arrays entlang ihrer Kanten aneinander anliegen.

Revendications

1. Groupement de pixels (10) comprenant :

une pluralité de lignes de sélection (ROW_SEL, COL_SEL) ;
une pluralité de lignes de signal (HSIG) ;
un groupement d'éléments de pixels, chaque élément de pixels comprenant :
un phototransducteur (12) ;

des moyens de commutation (16, 18) couplés entre le phototransducteur et l'une de ladite pluralité de lignes de signal ; dans lequel les moyens de communication réagissent à des signaux sur l'une de la pluralité de lignes de sélection en convoyant les signaux entre le phototransducteur et la ligne de signal ; caractérisé en ce que le groupement comprend de plus :

une pluralité de transistors configurables comprenant au moins un transistor configurable (20) dans chacun d'une pluralité des éléments de pixels, chaque transistor configurable comportant une pluralité de bornes, ces bornes étant adaptées pour établir des connexions entre des transistors respectifs de la pluralité de transistors configurables ; et

une pluralité de dispositifs de connexion (BUF_SIG, IN, OUT) qui connectent des bornes sélectionnées parmi les bornes de la pluralité de transistors configurables de façon à former un circuit multitransistor (710) qui est distribué parmi une pluralité des éléments de pixels dans le groupement de pixels ;

au moins certains desdits transistors configurables étant configurés de façon à exécuter des fonctions du circuit multitransistor qui sont indépendantes des fonctions des éléments de pixels contenant ces transistors.

2. Groupement de pixels selon la revendication 1, dans lequel la pluralité de lignes de sélection comprend une pluralité de lignes de sélection de colonne (COL_SEL) ;

   les moyens de commutation comprennent deux transistors série (16, 18), chacun d'entre eux réagissant à une ligne de sélection de colonne sélectionnée ; et

   la pluralité de dispositifs de connexion connectent des transistors sélectionnés parmi la pluralité de transistors configurables afin de réaliser, sous la forme dudit circuit multitransistor, un registre à décalage de sélection de colonne (710).

3. Groupement de pixels selon la revendication 1 ou 2, dans lequel le phototransducteur est un photodétecteur (12).

4. Groupement de pixels selon la revendication 3, comprenant de plus des moyens de stockage de charge (14) couplés en parallèle avec le photodétecteur pour conserver une charge électrique ayant une valeur qui est déterminée par l'intensité lumineuse.

5. Groupement de pixels selon la revendication 1, dans lequel la pluralité de lignes de sélection comprend une pluralité de lignes de sélection de rangée (ROW_SEL) et une pluralité de lignes de sélection de colonne (COL_SEL), le groupement de pixels comprenant de plus une pluralité de lignes auxiliaires (BUF_SIG, IN, OUT) ;

   le phototransducteur est un photodétecteur (12) ;

   les moyens de commutation réagissent à des signaux sur une ligne sélectionnée parmi les lignes de sélection de rangée et sur une ligne sélectionnée parmi les lignes de sélection de colonne en convoyant des signaux entre le photodétecteur et la ligne de signal prédéterminée ; et

   la pluralité de dispositifs de connexion comprend d'autres dispositifs de connexion qui connectent au moins un premier de la pluralité de transistors configurables (20) dudit circuit multitransistor à une ligne sélectionnée parmi lesdites lignes.

6. Elément de pixel selon la revendication 5, dans lequel la pluralité de lignes auxiliaires comprend une ligne de signal à mémoire tampon (BUF_SIG), dans lequel un deuxième de la pluralité de transistors configurables (20) est couplé entre la ligne de signal à mémoire tampon et une source de potentiel de référence (VDD), dans lequel le deuxième de la pluralité de transistors configurables réagit à la ligne de signal prédéterminée de telle sorte que, lorsque la ligne de signal prédéterminée est excitée, la ligne de signal à mémoire tampon achemine une version amplifiée du signal convoyé par la ligne de signal prédéterminée.

7. Groupement de pixels selon la revendication 5, dans lequel la pluralité de lignes de signal comprend une première pluralité de lignes de signal et une deuxième pluralité de lignes de signal, dans lequel un deuxième transistor au nombre d'au moins un de la pluralité de transistors configurables (20) est couplé entre l'une de la première pluralité de lignes de signal et l'une de la deuxième pluralité, dans lequel le deuxième transistor au nombre d'au moins un de la pluralité de transistors configurables réagit à la ligne de sélection de rangée sélectionnée de telle sorte que, lorsque la ligne de sélection de rangée sélectionnée est excitée, le deuxième transistor au nombre d'au moins un de la pluralité de transistors configurables couple la première de la première pluralité de lignes de signal à la première de la deuxième pluralité de lignes de signal.

8. Groupement de pixels selon la revendication 1, dans lequel le transducteur est un photodétecteur et le groupement

de pixels comprend de plus :

des moyens pour maintenir une charge (14) représentant la lumière détectée par le photodétecteur ;
des moyens, couplés aux moyens pour maintenir la charge et réagissant aux moyens de commutation, pour permettre l'accès à la charge maintenue ; et
des moyens pour coupler au moins l'un de la pluralité de transistors configurables à une pluralité d'autres transistors configurables afin de réaliser, sous la forme du circuit multitransistor, des circuits périphériques qui permettent successivement l'accès à la charge maintenue sur des éléments respectivement différents de la pluralité d'éléments de pixel.

9. Groupement de pixels selon l'une des revendications 1 à 5, 8, dans lequel chaque élément de pixel comprend un seul transistor configurable, qui est un transistor métal-oxyde-semiconducteur (MOS).

10. Groupement de pixels selon l'une quelconque des revendications 1 à 8, dans lequel chaque élément de pixel comprend deux transistors métal-oxyde-semiconducteur (MOS) configurables ayant des polarités de canal opposées.

11. Groupement de pixels selon la revendication 10, dans lequel les deux transistors MOS configurables dans une cellule sont configurés sous la forme d'un inverseur métal-oxyde-semiconducteur complémentaire (CMOS) et les dispositifs de connexion sont utilisés pour connecter les inverseurs dans des éléments sélectionnés parmi les éléments de pixel à des transistors individuels parmi les transistors configurables dans d'autres éléments sélectionnés parmi les éléments de pixel afin de former un registre à décalage de sélection de colonne.

12. Matrice d'une pluralité de groupements de pixels (920) qui sont chacun comme spécifié dans l'une quelconque des revendications précédentes, les groupements étant interconnectés (926, 928).

13. Matrice selon la revendication 12, dans laquelle les groupements sont en butée le long des bords de ceux-ci.

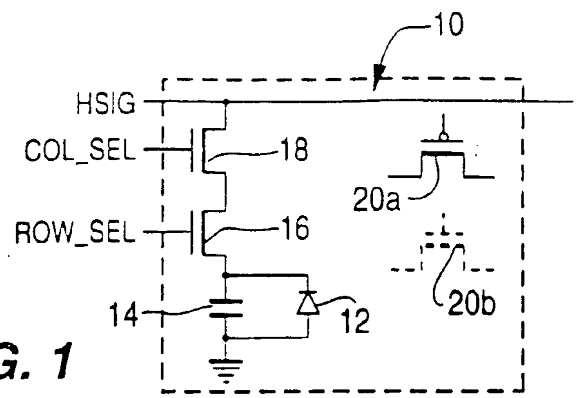


FIG. 1

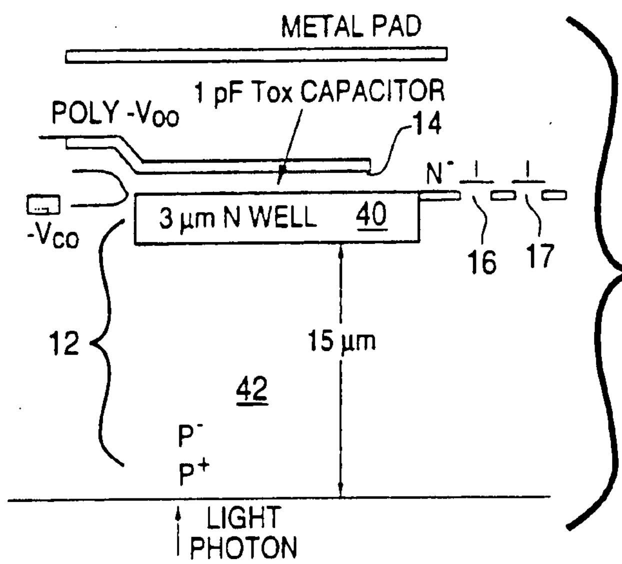


FIG. 2

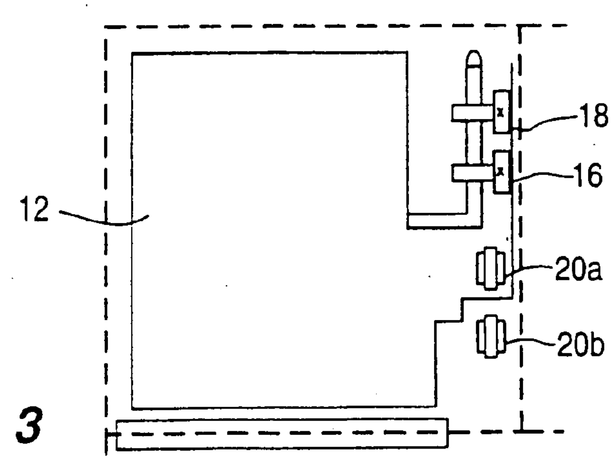


FIG. 3

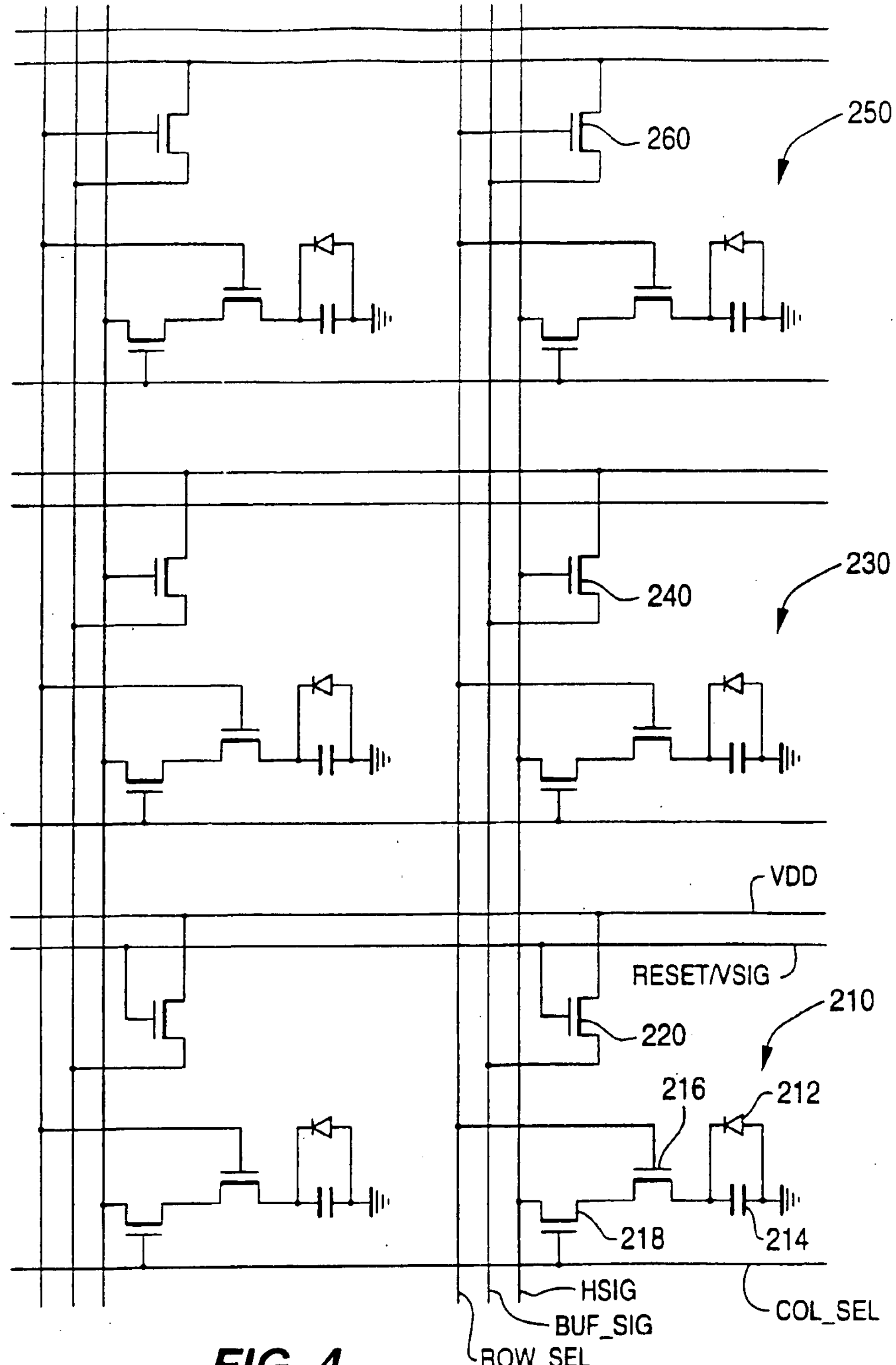

250
260
230
240
VDD
RESET/VSIG
210
220
216
212
218
214
HSIG
BUF_SIG
COL_SEL
ROW_SEL

FIG. 4

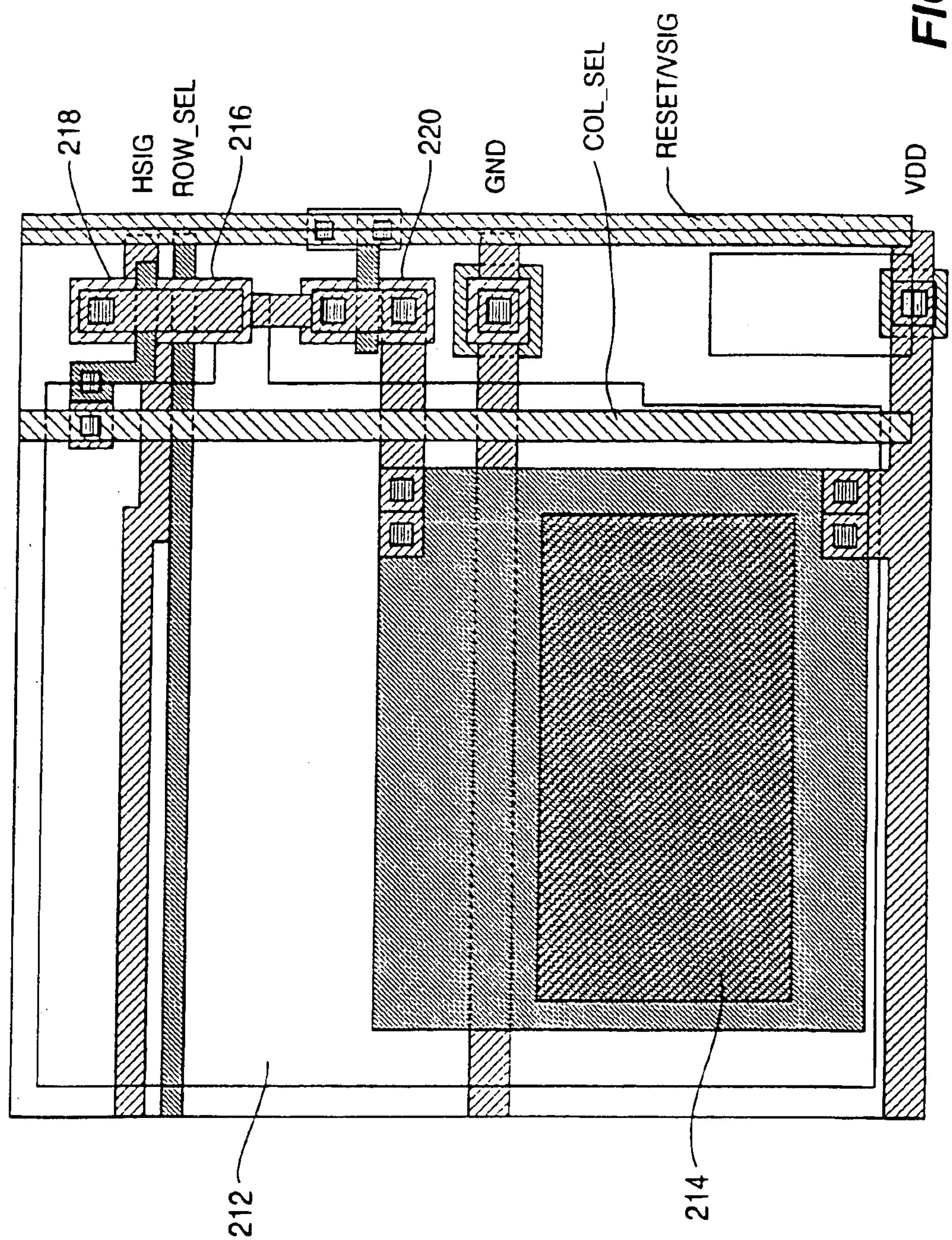
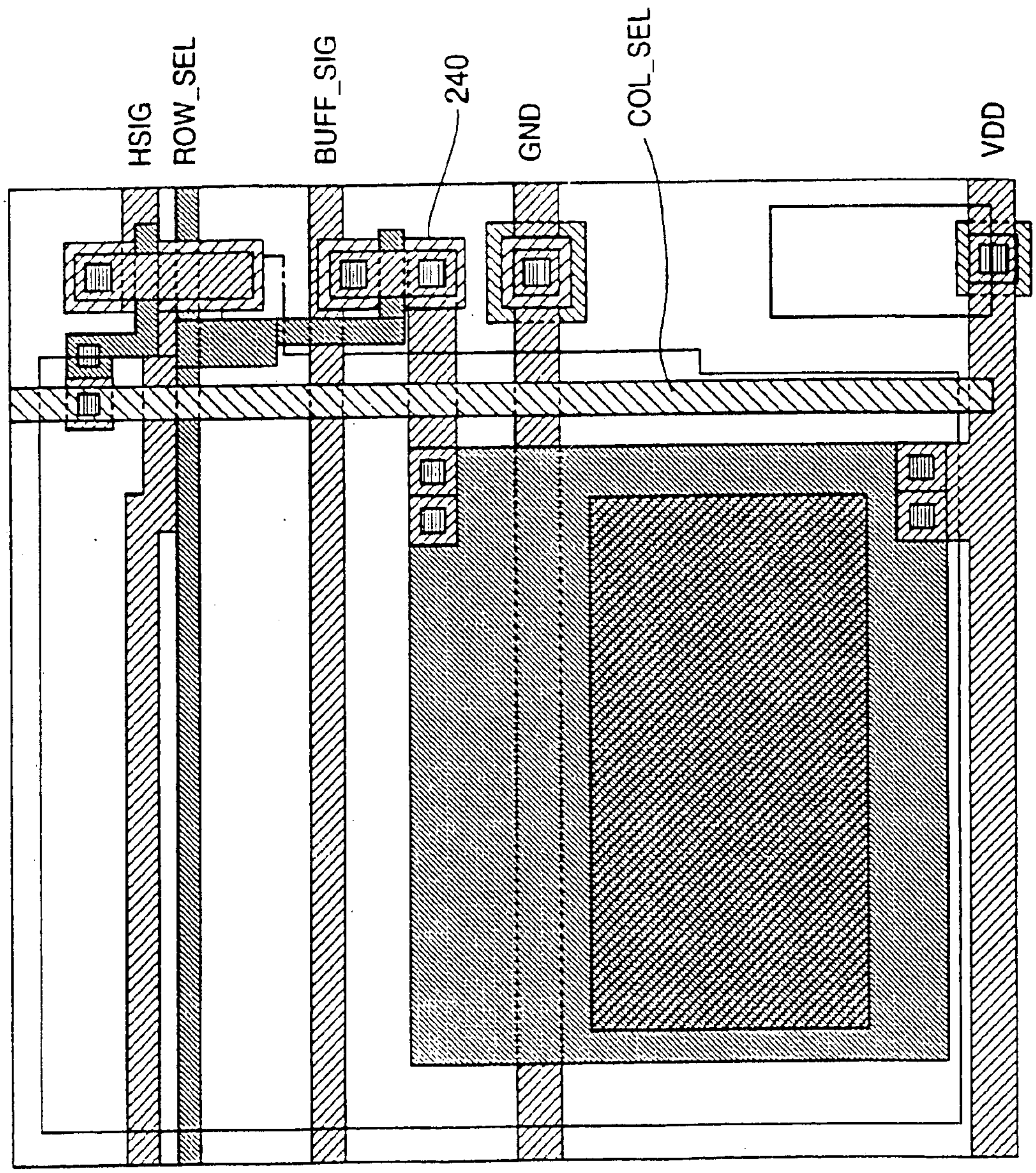


FIG. 5

FIG. 6



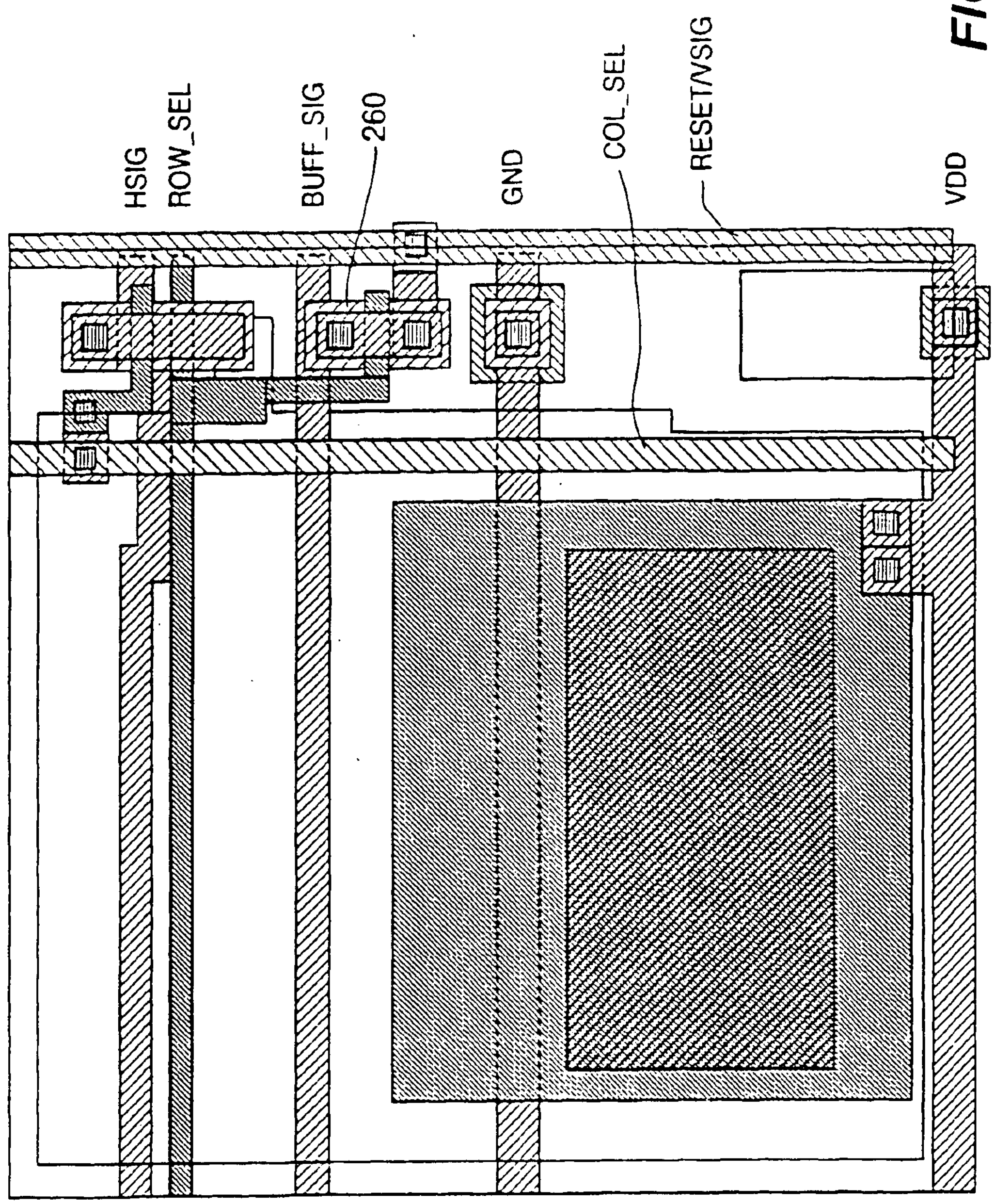


FIG. 7

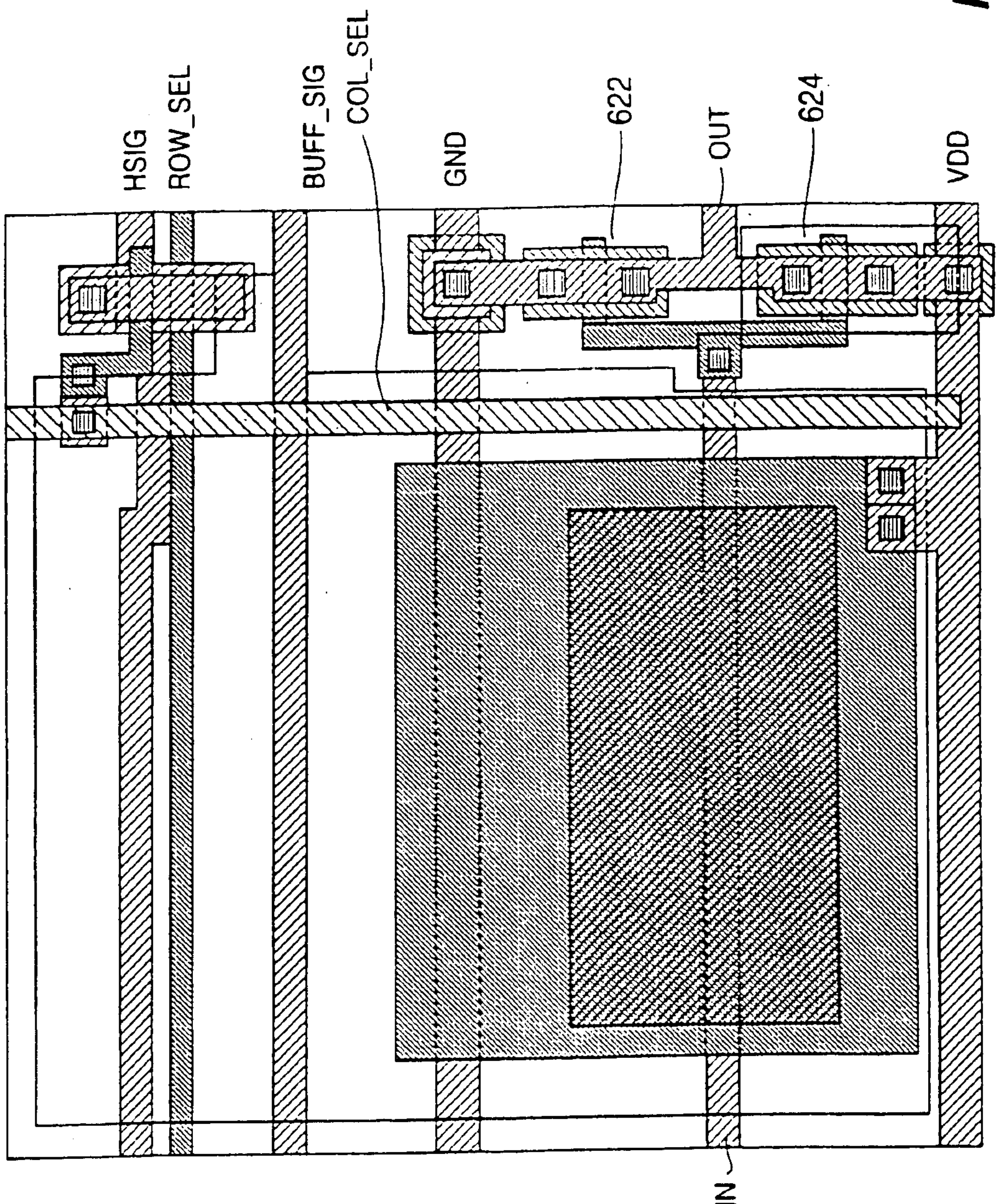
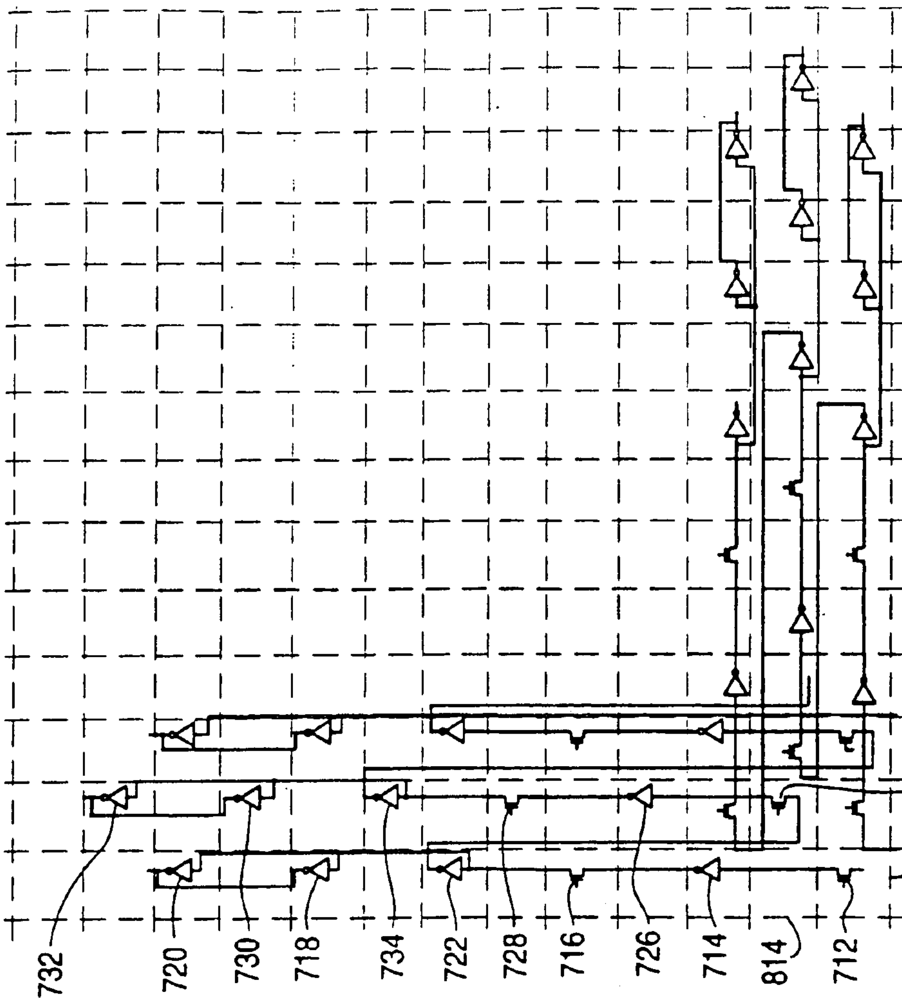


FIG. 8



810

FIG. 10

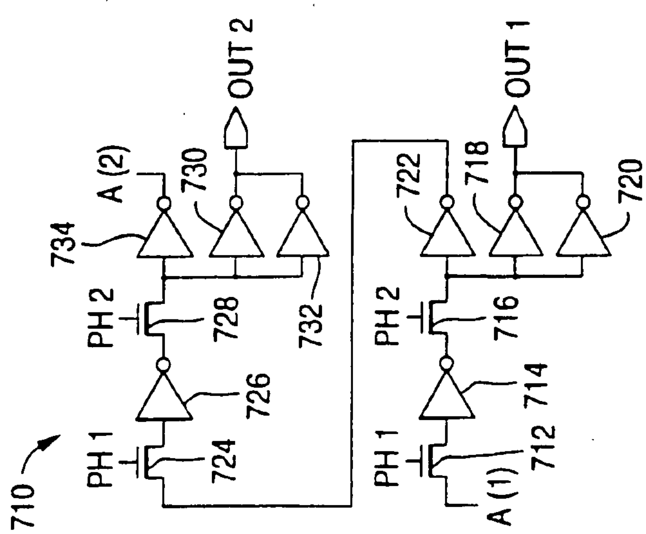


FIG. 9

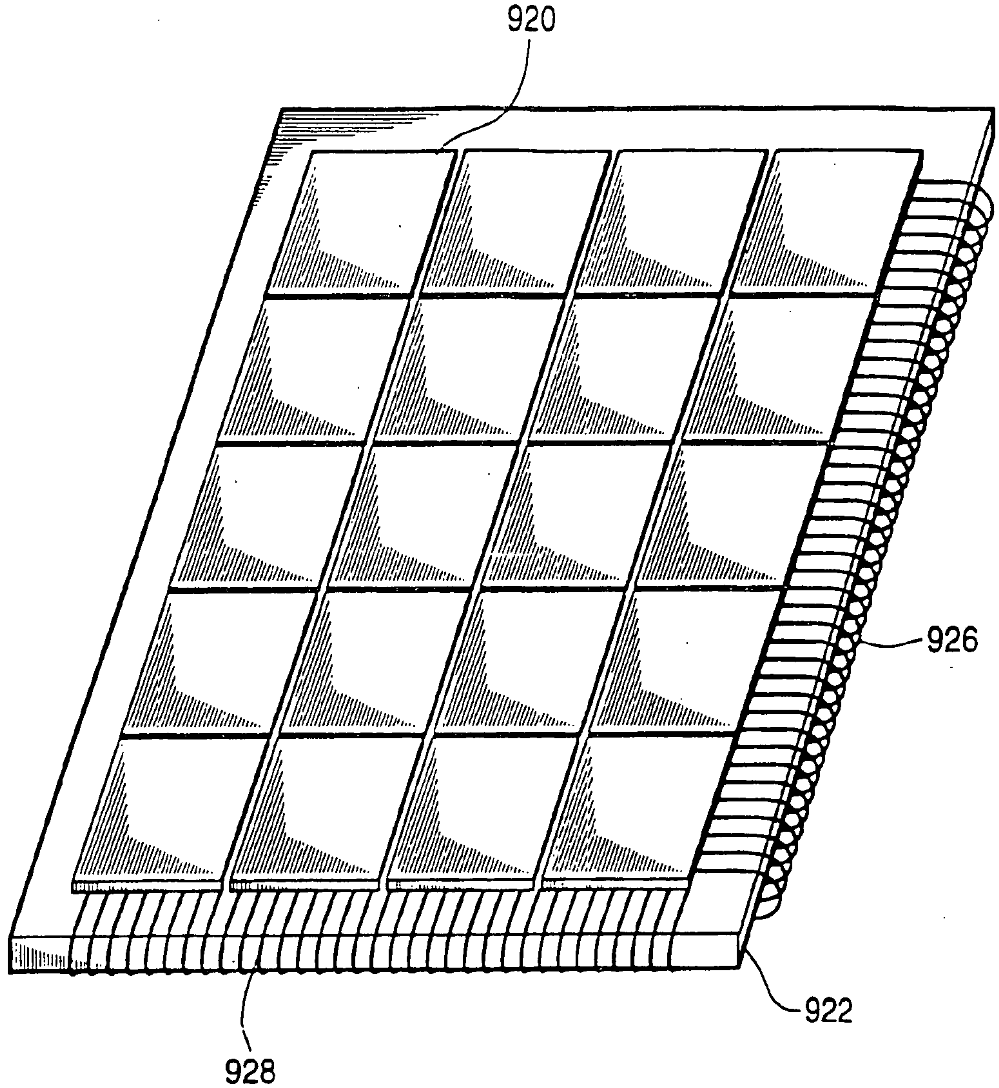
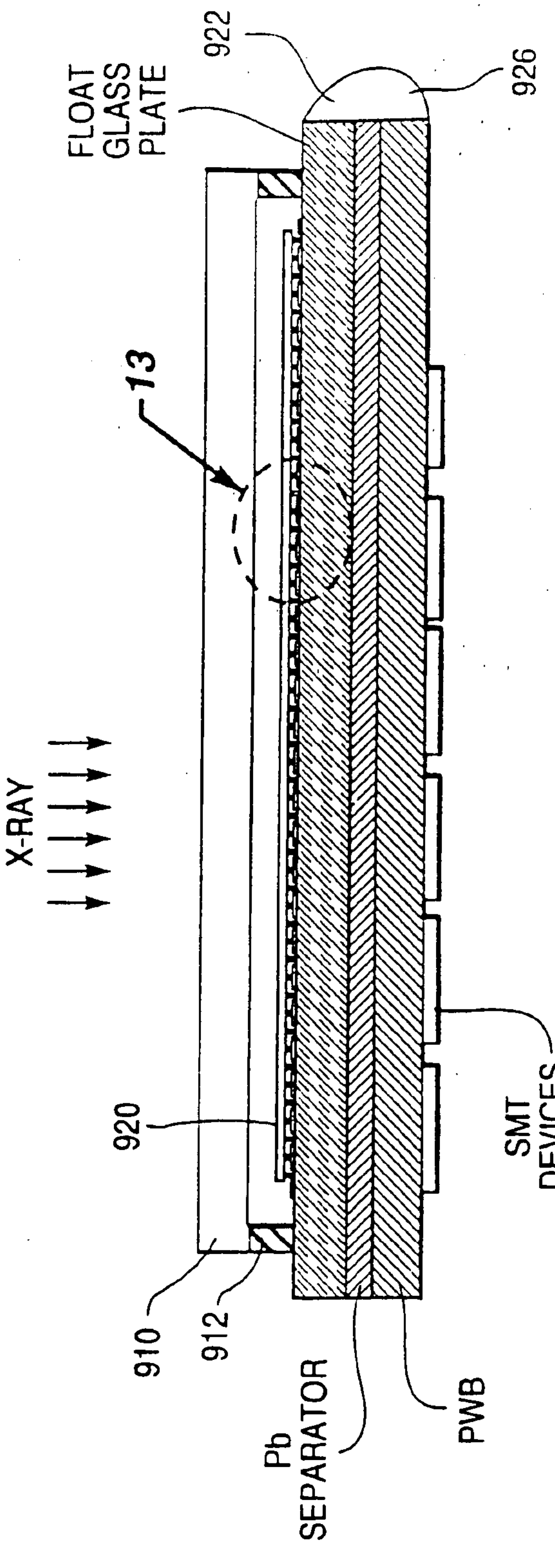
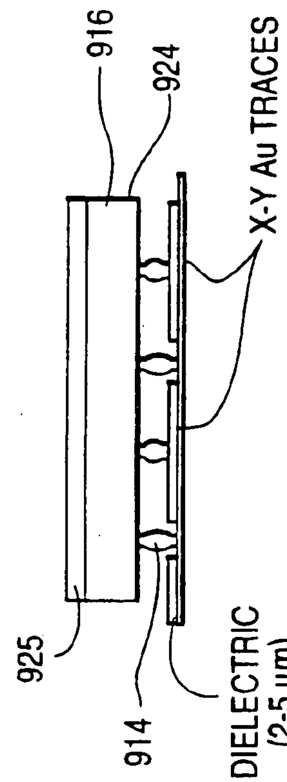


FIG. 11



922
926
FLOAT GLASS PLATE
13
X-RAY
920
910
912
Pb SEPARATOR
PWB
SMT DEVICES

FIG. 12



916
924
X-Y Au TRACES
925
914
DIELECTRIC (2-5 μm)

FIG. 13